In the specification:

On page 1, line 2, after the Title of the Invention add the following:

This application is a divisional of U.S. Patent Application Serial No. 10/078,861, now U.S. Patent 6,734,090.

In the claims:

Claims 1 - 8 (Canceled).

9. (Currently amended) An edge seal around the periphery of an integrated circuit device comprising:

~~a.~~ a semiconductor substrate;

~~b.~~ a layer of low-k dielectric material over the semiconductor substrate~~, the layer of dielectric material comprising a low-k dielectric material~~;

a layer of hard material over or under the layer of low-k dielectric material, the layer of hard

material selected from the group consisting of a dielectric material and a hard mask material; and

an edge seal structure around the periphery of an integrated circuit device comprising:

~~c.~~ a metallic wall of a high conductivity metal in the layer of dielectric material and in the layer of hard material; and

~~d.~~ a layer of insulation material between the metallic wall and the low-k dielectric material and between the metallic wall and the layer of hard material, wherein the insulation material and low-k dielectric material are different materials.

10. (Original) The edge seal of claim 9 wherein the low-k dielectric material comprises SiLK or fluoridized polyimide.

11. (Currently amended) The edge seal of claim 9 wherein the layer of hard material ~~dielectric material~~ comprises a bottom layer on the semiconductor substrate under the low-k dielectric material ~~, the low-k dielectric material on the bottom layer~~ and a top moisture barrier on the low-k dielectric material.

12. (Original) The edge seal of claim 9 wherein the insulation material is selected from the group consisting of $SiO_2$, SiC, $Si_3N4$, $Al_2O_3$, diamond like carbon, polyimide and combinations thereof.

13. (Original) The edge seal of claim 9 further comprising a barrier layer between the metallic wall and the insulation material wherein the barrier layer is selected from the group consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium, titanium nitride, tungsten silicide and combinations thereof.

14. (Original) The edge seal of claim 9 wherein the high conductivity metal is copper.

15. (Original) The edge seal of claim 9 wherein the thickness of the insulation material is 0.05 microns to 0.5 microns.

16. (Currently amended) An edge seal around the periphery of an integrated circuit device comprising:

~~a.~~ a semiconductor substrate;

~~b.~~ a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material; and

an edge seal structure around the periphery of an integrated circuit device comprising:

~~c.~~ a metallic wall of a high conductivity metal in the layer of dielectric material; and

~~d.~~ a layer of insulation material between the metallic wall and the dielectric material, wherein the insulation material and dielectric material are different materials, ~~The edge seal of claim 9~~ wherein there are two spaced-apart metallic walls physically connected by a metallic cross piece in the at least one layer of dielectric material, each of the metallic walls comprising two spaced-apart sides, and there is a layer of insulation material between the dielectric material and each of the metallic walls with each layer of insulation material being of a different material than the dielectric material.

Claim 17 (Canceled).

18. (Currently amended) An edge seal around the periphery of an integrated circuit device comprising: